

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,849,493 B2
DATED : February 1, 2005
INVENTOR(S) : Shubneesh Batra et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1,

Line 37, replace "a is semiconductive wafer fragment 10 is shown at a" with
-- a semiconductive wafer fragment 10 is shown at a --.

Column 2,

Line 30, replace "52, 54, 56 and 58 within openings 22, 24, 26, 29 and 30," with
-- 52, 54, 56 and 58 within openings 22, 24, 26, 28 and 30, --.

Column 7,

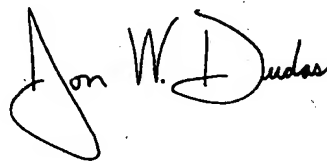
Line 65, replace "layer joining the upper layer at an interlace, the" with
-- layer joining the upper layer at an interface, the --.

Column 8,

Line 61, replace "interlace is elevationally proximate the uppermost surface of" with
-- interface is elevationally proximate the uppermost surface of --.

Signed and Sealed this

Twenty-eighth Day of March, 2006

A handwritten signature in black ink, appearing to read "Jon W. Dudas", is written over a faint rectangular stamp.

JON W. DUDAS
Director of the United States Patent and Trademark Office